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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/818,313	03/27/2001	Chii-Hwang Chang	67,200-392	1765

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EXAMINER	
MOORE, KARLA A	

ART UNIT	PAPER NUMBER
1763	

DATE MAILED: 03/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/818,313	CHANG ET AL.	
	Examiner	Art Unit	
	Karla Moore	1763	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 13-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 13-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1-6 and 13-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,201,999 to Jevtic.

4. Jevtic discloses a method for operating a multi-chamber fabrication tool substantially as claimed and comprising: providing a multi-chamber fabrication tool comprising a series of chambers (Figure 1, column 2, rows 13-20 and 62-65); first defining for each chamber within the series of chambers a minimum of one fabrication process to provide a series fabrication processes corresponding to the series of chambers prior to processing a substrate within said series of chambers (column 2, row 66 through column 5, row 9), wherein at least one fabrication process is undertaken in more than one chamber (column 5, rows 11-21; In the disclosure, a "stage" is defined as set of chambers which correspond to the same process. Clearly, a process that can be undertaken in more than one chamber is contemplated) and at least one chamber has defined therein more than one fabrication process (column 5, rows 48-51; In the disclosure, a trace (process map) is said to be knotted if there is a chamber whose name appears

more than once in the trace. Clearly, a chamber performing more than one process is contemplated); then selecting the at least one chamber for processing the substrate while employing the at least one fabrication process which is undertaken within more than one chamber, the at least one chamber selected to optimize utilization of the multi-chamber fabrication tool (column 14, row 57 through column 15, row 7); then processing within the multi-chamber fabrication tool the substrate while employing the at least one fabrication process which is undertaken in more than one chamber.

5. However, Jevtic fails to explicitly teach that a chamber defined to be used for the process undertaken in more than one chamber is also a chamber that has more than one process defined therein.

6. According to Jevtic, in a method of using the multi-chamber tool, what is of most importance is finding a schedule that produces the highest throughput (abstract and column 14, row 57 through column 15, row 7). The highest throughput schedule is found by producing every possible processing sequence and then determining which is best. Jevtic discloses each of the situations above as part of a processing method. In a method using the scheduler as disclosed in Jevtic and comprising both of the processing situations above, there would be at least one schedule produced containing both situations because the scheduling routine produces every possible schedule. Thus, the two situations above, although not explicitly disclosed as such, would be part of a chosen processing sequence, when they are found to provide optimal throughput.

7. It would have been obvious to one of ordinary skill in the art at the time the Applicant's invention was made to have provided a method comprising selecting a chamber defined to be used for a process undertaken in more than one chamber, wherein that chamber also has more than one process defined therein, for processing using a scheduling routine as disclosed in Jevtic in order to optimize throughput as taught by Jevtic.

8. With respect to claims 2 and 14, the substrate is employed within a microelectronic fabrication selected from the group consisting of integrated circuit microelectronic fabrications, ceramic substrate microelectronic fabrications, solar cell optoelectronic microelectronic fabrications, sensor image array

optoelectronic microelectronic fabrications and display image array optoelectronic microelectronic fabrications (column 2, rows 16-25).

9. With respect to claims 3 and 15, the series of chambers comprises at least about 4 chambers (see Figure 1).

10. With respect to claims 4 and 16, the series of fabrication processes is selected from the group consisting of vacuum etch processes, vacuum deposition processes and vacuum implantation processes (see 26-30 and 61-62, where it is disclose that the system comprises load lock chambers, which are for introducing substrates into a vacuum system and where it is also disclosed that a vapor deposition process is performed).

11. Claims 5-6 and 17-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jevtic as applied to claims 1-4 and 13-16 above, further in view of U.S. Patent No. 6,519,498 to Jevtic et al. (2).

12. Jevtic discloses the invention substantially as claimed and as described above.

13. However, Jevtic fails to explicitly disclose the method further comprises defining a series of chamber constraints for the series of chambers; defining a series of process constraints for the series of processes; and defining a series of substrate constraints for the substrate. Examiner notes that all manufacturing methods, particularly multi-chamber processes, would clearly be subject to the above constraints without them being explicitly defined in a processing method. This is because for any given piece of multi-chamber equipment there will be a specific number of process chambers (i.e. chamber constraints) associated with the equipment, a specific number of processes that the chambers are capable of (i.e. process constraints), and a specific number of substrates to be presented for processing at any given time (i.e. substrate constraints). Jevtic further fails to explicitly teach a series of chamber constraints, a series of process constraints and a series of substrate constraints is prioritized through use of an algorithm when selecting the chamber within which is processed the substrate.

14. Jevtic et al. (2) teach a method for determining and selecting an optimal processing schedule/routine in a multi-chamber processing tool comprising providing a plurality of ranked input parameters (constraints) and executing an algorithm using the parameters to determine expected

processing results using the parameters. The outputted results for different inputted parameters can be compared and an optimal schedule/routine can be selected based on the comparison(s) (abstract and Figure 3).

15. It would have been obvious to one of ordinary skill in the art at the time the Applicant's invention was made to have provided a method for determining and selecting an optimal processing schedule/routine in a multi-chamber processing tool comprising providing a plurality of ranked input parameters (constraints) and executing an algorithm using the parameters in Jevtic in order to determine expected processing results using the parameters, therefore enabling comparisons and selection of an optimal schedule/routine as taught by Jevtic et al. (2).

Response to Arguments

16. Applicant's arguments with respect to claims 1-6 and 13-18 have been considered but are moot in view of the new ground(s) of rejection. Jevtic and Jevtic et al. teach a method comprising defining a wafer processing routine prior to the start of wafer processing, as recited in the newly amended claims.

Conclusion

17. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Karla Moore whose telephone number is 571.272.1440. The examiner can normally be reached on Monday-Friday, 8:30am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Parviz Hassanzadeh can be reached on 571.272.1435. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Karla Moore
Patent Examiner
Art Unit 1763
9 March 2006